UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,076,756 B2
APPLICATION NO. : 10/701249
DATED : July 11, 2006
INVENTOR(S) : Junji Ichimiya

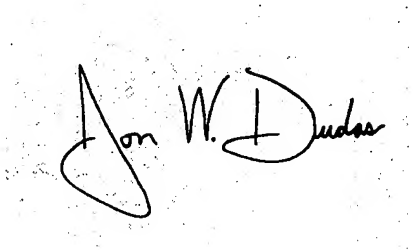
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Replace the Title section on the cover page of the patent, with the following:

-- (54) LAYOUT DESIGN METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT, WITH HIGH INTEGRATION LEVEL OF MULTILEVEL METALLIZATION--

Signed and Sealed this

Fourteenth Day of August, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office